Use Spice to analyze DRL in an ECG front end

Matthew Hann, Texas Instruments - January 5, 2012

ECG (electrocardiography) is the science of converting the ionic depolarization of the heart to a measurable electrical signal for analysis. One of the most common challenges in the design of analog electronics interfaces to the electrodes or to patients is optimization of the DRL (driven-right-leg) circuit, which is often added to biological-signal amplifiers to reduce common-mode interference and to increase performance and stability. Using Spice to help in this effort can greatly simplify the process.

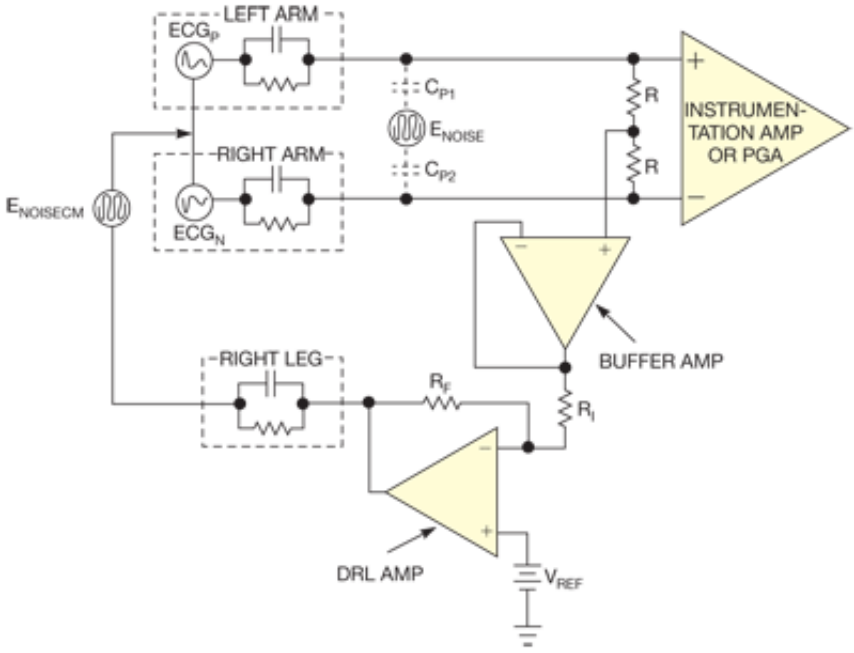

Figure 1 The positive and the negative ECG sources, ECG_P and ECG_N, split to show how the DRL amplifier provides the common reference point for a portion of the ECG signal that the positive and negative inputs of the instrumentation amplifier sees.

In an ECG front end, the DRL amplifier provides a common electrode bias at the reference voltage, V_{REF}, and feeds back the inverted common-mode noise signal, $e_{NOISECM}$, to reduce the overall noise seen at the inputs of the instrumentation amplifier's gain stage. The positive and negative ECG sources, ECG_P and ECG_N, are split to show how the DRL amplifier provides the common reference point for a portion of the ECG signal that is seen at the positive and the negative inputs of the instrumentation amplifier (**Figure 1**).

The parallel RC (resistance/capacitance) combination for the left arm, the right arm, and the right leg represents the lumped passive-electrode connection impedances, which are 52 kΩ and 47 nF. Assuming that e_{NOISE} couples parasitically into the inputs, the feedback of $e_{NOISECM}$ will reduce the overall noise signal at each input, leaving the task of either externally filtering the residual noise or having the CMRR reject the instrumentation amplifier's common-mode noise.

Figures 2, **3**, and **4** show the variation in CMRR of the common-mode test circuit with the varying gain of the DRL amplifier. These plots show that you can achieve the best low-frequency CMRR with no feedback resistor, yielding infinite gain. In reality, however, eliminating the dc path, setting RF to a high value, or using both of these methods may be impractical for applications that require the linear operation of the DRL amplifier when one of the input amplifier's leads is removed.

TALKBACK

We would love your feedback!
Post a comment below.

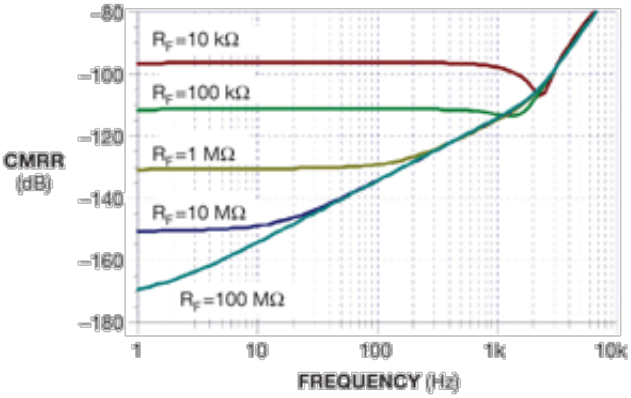

Figure 3 Eliminating the dc path, setting RF to a high value, or using both of these methods may be impractical for applications that require linear operation of the DRL amplifier when you remove one of the input amplifier leads.

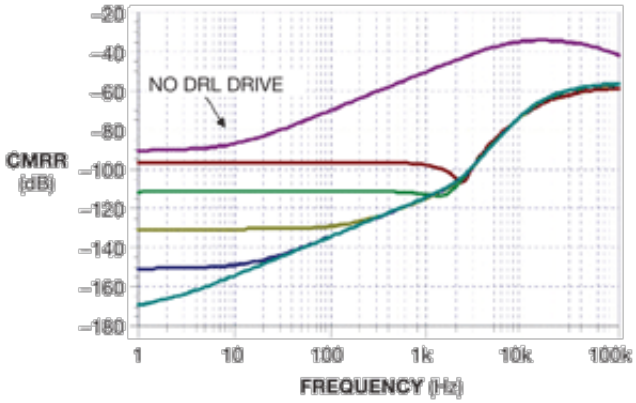

Figure 4 Gain is higher in circuits with no DRL drive.

Once you determine the gain of the DRL amplifier, the next step is to inject a small signal step in the loop and monitor the output response (**Figure 5**). In this case, the response shows a strong output oscillation, indicating instability in the loop (**Figure 6**). The dominant feedback path causing this instability is the feedback path for the body, the electrode, and the instrumentation-amp feedback path around the DRL amplifier. A test circuit allows you to separate and analyze the feedback and the open-loop-gain curve of the DRL amplifier on a bode plot (**Figure 7**).

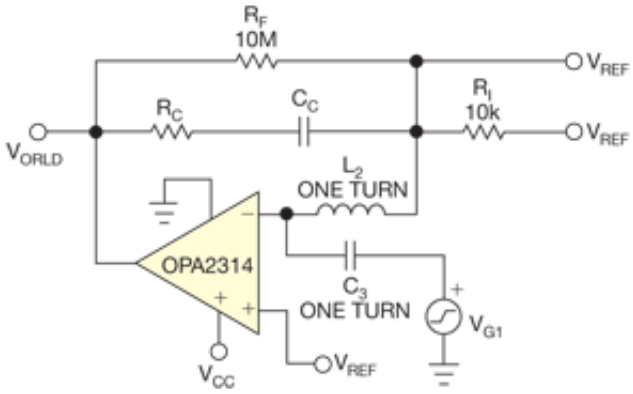

Figure 8 Without an external compensation network, the beta-distribution curve approaches the open-loop-gain curve at a rate of closure greater than 20 dB per decade, indicating instability.

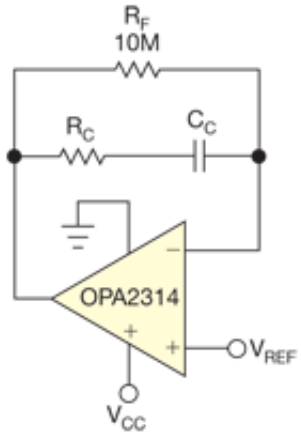

Figure 9 Add series resistor R_C and capacitor C_C in the local feedback of the DRL amplifier.

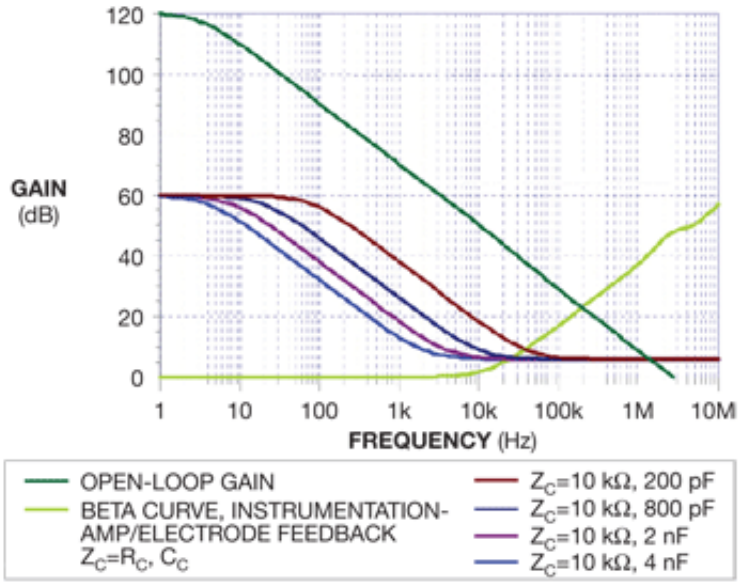

Figure 10 The result for the simulation in Figure 7 is represented by the beta curve.

Without an external compensation network, the beta-distribution curve approaches the open-loop-gain curve at a rate of closure greater than 20 dB per decade, indicating instability. To address this issue (**Figure 8**), add series resistor R_C and capacitor C_C (**Figure 9**) in the local feedback of the DRL amplifier. Z_C then becomes the dominant feedback path between 20 and 30 kHz. The result for the simulation in **Figure 7** is represented by the beta (feedback) curve in **Figure 10**. Figure 11 shows the full circuit of the DRL with compensation. **Figure 12** shows the compensated beta-curve plots, employing variations in R_C and C_C. The overall beta curve intersects the open-loop-gain curve with a rate of closure that is 20 dB per decade or less and a loop gain with a phase margin greater than 45° (**Figure 13**).

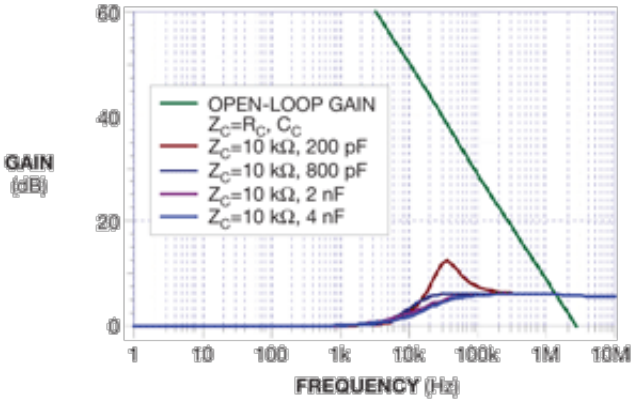

Figure 12 The compensated beta-curve plots employ variations in R_C and C_C.

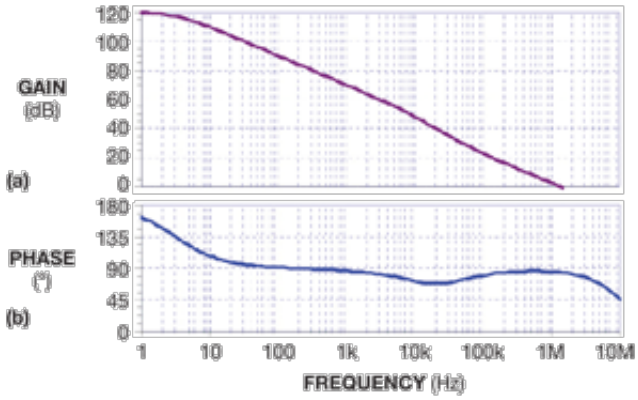

Figure 13 The overall beta curve intersects the open-loop-gain curve with a rate of closure that is 20 dB per decade or less and a loop gain (a) with a phase margin greater than 45° (b).

Spice can be a useful tool to quickly help analyze and optimize the performance and stability of the DRL's front-end circuitry. Keep in mind that the simulation is only as good as the models, so it is important to correctly model key specifications, such as noise, open-loop gain, open-loop output impedance, and CMRR versus frequency, before analysis and design.

Acknowledgment

This article originally appeared on EDN*'s sister site,* Planet Analog.

Author's biography

Matthew William Hann is a precision-analog-applications manager at Texas Instruments. He has more than a decade of product expertise, which includes temperature sensors, difference amplifiers, instrumentation amplifiers, programmable-gain amplifiers, power amplifiers, and TI's line of ECG analog-front-end devices. Through his role as an applications engineer, Hann has developed a focused expertise on the design of analog front ends for medical applications, such as ECGs, electroencephalograms, electromyograms, blood-glucose monitoring, and pulse oximetry. Hann received a bachelor's degree in

electrical engineering from the University of Arizona—Tucson. You can reach him at ti_matthann@list.ti.com.